MULTIPLEXER CIRCUIT AND ANALOGUE-TO-DIGITAL CONVERTER

The invention relates to a multiplexer circuit according to the preamble of claim 1 and to an analogue-to-digital converter (ADC)comprising such a multiplexer circuit.

In monolithic IC's transmission gates can be used for multiplexer circuits. They are suitable to select one of several analogue input channels to connect the selected channel, for example, to an ADC circuit on chip. Multiplexer circuits built with transmission gates implemented in monolithic IC's with MOS (metal oxide semiconductor) type circuits are known from CMOS Digital Integrated Circuits, Analysis and Design, S.M. Kang, Y. Leblebici, McGRAW-HILL INTERNATIONAL EDITIONS, ISBN 0-07-038046-5, page 274 and from Principles of CMOS VLSI Design, A System Perspective, second edition ADDISON WESLEY, N.H.E., Weste, K. Eshraghian, ISBN 0-201-53376-6, pages 17, 304.

An example of a conventional multiplexer circuit 1 comprising transmission gates is shown in Fig. 5. The multiplexer circuit 1 comprises at least two input channels IN_0, IN_1 which are connected with a common output channel 2. Of course, a plurality of input channels IN_0, IN_1, IN_2,... IN_i may be provided in the multiplexer circuit. For selecting one of said analogue input channels IN_0, IN_1 the multiplexer circuit comprises transmission gates FT_0, FT_1 between the input channel IN_0, IN_1 and the output channel 2, respectively. The

multiplexer can select one of the two input channels IN_0, IN_1 by select signals $SELECT_0$, $\overline{SELECT_0}$, $SELECT_1$, $\overline{SELECT_1}$ generated by a decoder circuit 10. The decoder circuit generates a select signal $SELECT_0$, $SELECT_1$ and an inverted select signal $\overline{SELECT_0}$, $\overline{SELECT_1}$ for each input channel IN_0, IN_1, respectively, which are applied to the corresponding transmission gates FT_0, FT_1. The decoder circuit is a n to 2^n decoder ($i = 2^n$), which ensures that only one of the select signals $SELECT_0$ to $SELECT_i$ becomes true while the others are false, i.e. only one channel is open while the others are closed. In the example according to Fig. 4 the channel IN_1 is selected i. e. the transmission gate FT_1 is open, whereas the channel IN_0 is not selected and the transmission gate FT_0 is closed. Analog voltages U_1, U_2 are applied to the input channels IN_0, IN_1, respectively. The voltage at the output channel 2 is indicated as U_{out}. The transmission gates FT_0, FT_1 are known CMOS transmission gates comprising p channel and n channel transistors having threshold voltages V_{THp} and V_{THn}, respectively. The multiplexer circuit is operated with a power supply voltage V_{CC} and V_{SS} is the ground potential 0V.

The operation of the multiplexer circuit is as follows. In a normal operation condition the following input voltage conditions are applied:

$$U_1 = [V_{SS}; V_{CC}]$$
$$U_2 = [V_{SS}; V_{CC}].$$

That means the level of the input voltages U_1, U_2 is between the power supply voltage level V_{CC} and V_{SS}.

Under these conditions the transmission gates FT_0 and FT_1 operate as ideal switches. Since the transmission gate FT_0 is closed, the voltage U_{out} is equal to U_2:

$$U_{out} = U_2.$$

No current will flow in the multiplexer circuit, i.e. the current in the channels IN_0 and IN_1 is 0, respectively:

$$I_{in1} = 0$$
$$I_{out} = 0.$$

In case of an over or an under voltage applied to an input channel which is not selected i. e. which is not active a current will flow through the active channel. This is the under/over voltage operation condition. The following input voltage conditions are considered as under and over voltage conditions:

Under voltage:

$$-V_{THn} + V_{SS} \leq U_1 \leq V_{SS}.$$

Over voltage:

$$V_{CC} \leq U_1 \leq V_{CC} + |V_{THp}|,$$

The voltage U_2 is:

$$U_2 = [V_{SS}; V_{CC}].$$

Under these conditions the transmission gate FT_0 in channel IN_0 does not work as an ideal switch any more. Due to "weak inversion" and the pn-diode structures of the CMOS transistors a current flows between IN_0 and IN_1.

$$\begin{vmatrix} I_{in} \\ I_{out} \end{vmatrix} \geq 0$$

I_{out} creates a voltage drop at the resistance of the transmission gate FT_1 in channel IN_1 and the output resistance of the source of U_2. Therefore, U_{out} is not equal to the input voltage U_2 any more. Depending on the desired accuracy of the analogue signal this will be a problem.

In particular for multiplexer circuits used in ADC's a noise at the injection source leads to worse accuracy, which makes the conversion results unusable (e.g. in case of an 8-bit ADC the absolute accuracy becomes 10-11 LSB instead of +/-2 LSB). External over/undervoltage protection circuits are required in order to be able to use such ADC's.

It is an object of the invention to provide a multiplexer circuit and an analogue-to-digital converter having an improved accuracy with respect to the output of an analogue input signal.

The object is solved by a multiplexer circuit according to claim 1 and by an analogue-to-digital converter according to claim 12. Further developments of the invention are described in the dependent claims.

Embodiments of the invention will be explained with reference to the accompanying drawings.

Fig. 1 shows a multiplexer circuit according to a first embodiment of the invention.

Fig. 2 shows a multiplexer circuit according to a second embodiment of the invention.

Fig. 3 shows a multiplexer circuit according to the second embodiment of the invention more in detail.

Fig. 4 shows a multiplexer circuit according to a further embodiment of the multiplexer circuit of Fig. 2.

Fig. 5 shows an example of a conventional multiplexer circuit.

A first embodiment of the multiplexer circuit according to the invention is shown in Fig. 1. Parts which are the same as in the conventional multiplexer circuit according to Fig. 4 are

designated with the same reference signs and the description thereof will not be repeated.

The multiplexer circuit according to this embodiment comprises a first transmission gate FT_0, FT_1, for each channel respectively, and a second transmission gate ST_0, ST_1 for each channel. The output of the first transmission gate FT_0, FT_1 in each channel is connected with the input of the second transmission gates ST_0, ST_1, respectively. The output of the second transmission gate ST_0 and ST_1 is connected with the output channel 2. The second transmission gate ST_0, ST_1 are controlled by the same select signals $SELECT_0$, $\overline{SELECT_0}$ and $SELECT_1$, $\overline{SELECT_1}$ as the first transmission gates FT_0, FT_1.

A bypass circuit in form of an NMOS transistor 20, 21 is provided for each analogue input channel IN_0, IN_1. Each NMOS transistor 20, 21 is connected with its drain to a node 30 31. Each node 30, 31 is connected with the output of the first transmission gate FT_0, FT_1 and the input of the second transmission gate ST_0, ST_1, respectively. The source of each NMOS transistor 20, 21 is connected with the ground potential level V_{SS}. The gate of each NMOS transistor receives the inverted select signal $\overline{SELECT_0}$, $\overline{SELECT_1}$, respectively, which is generated by the channel decoder 10. In this embodiment the NMOS transistors are controlled by the same select signal as the PMOS transistor of the transmission gates.

In the example according to Fig. 1 the channel IN_1 is selected and the first transmission gate FT_1 and the second transmission gate ST_1 are both open. Since the NMOS transistor 21 receives the inverted select signal $\overline{SELECT_1}$ on its gate, the NMOS transistor 21 is switched off for the selected channel IN_1. The channel IN_0 is not selected and therefore, the first transmission gate FT_0 and the second transmission gate ST_0 are both closed. Since the NMOS transistor 20 receives the inver-

ted select signal $\overline{SELECT_0}$ on its gate, the NMOS transistor 20 is switched on for the not selected channel IN_0.

In operation the select signals are applied to the transmission gates such that the input channel IN_1 is selected by opening the first transmission gate FT_1 and the second transmission gate ST_1 by the select signal $SELECT_1$ ($SELECT_1 = 1$). The other input channel IN_0 is not selected by closing the first transmission gate FT_0 and the second transmission gate ST_0 by applying the select signal $SELECT_0$ ($SELECT_0 = 0$).

In case the voltage U_1 applied to the first input channel IN_0 has an over voltage i.e.

$$V_{CC} \leq U_1 \leq V_{CC} + |V_{THp}|,$$

a current I_{in1} flows through the first transmission gate FT_0 to node 30. Since the NMOS transistor 20 is switched on by the select signal $\overline{SELECT_0}$, the current I_{in1} is bypassed through the NMOS transistor 20 to ground. The potential at node 30 is (due to being pulled down by NMOS transistor 20) in the range of $[0, V_{CC}]$. Therefore, the transmission gate ST_0 operates as an ideal switch, i.e. closes perfectly. Therefore, the selected input channel IN_1 is not influenced by the over voltage on the first input channel IN_0. The output voltage U_{out} is equal to U_2.

Without changing the circuit in Fig. 1 the NMOS transistor 20 pulls an undervoltage $-V_{TH,N} < U_1 < 0$ at the input to a potential in the range of $[-V_{TH,N}, 0]$ at node 30. This is enough to switch the transmission gate ST_1 off and to avoid influence to the analogue input. Hence, the NMOS transistor is a measure against under voltage. However, the bypass behaviour of the NMOS transistor for over voltage condition is better than for under voltage condition.

Fig. 2 shows an embodiment of a multiplexer circuit in order to bypass the current for over or under voltage conditions. In

the embodiment according to Fig. 2 parts which are equal to parts of the embodiment according to Fig. 1 are described with the same reference signs. The multiplexer circuit according to Fig. 2 comprises a pull-down bypass circuit 50, 51 in each channel IN_0, IN_1 and in addition a pull-up bypass circuit 60, 61. The pull-down bypass circuit 50, 51 is connected between a node 70, 71 and V_{SS} level and the pull-up bypass circuit 60, 61 is connected between the node 70, 71 and V_{CC} level, respectively.

The multiplexer circuit according to Fig. 2 also comprises two operation conditions: In the normal operation condition the following input voltage conditions are applied:

$$U_1 = [V_{SS};\ V_{CC}]$$
$$U_2 = [V_{SS};\ V_{CC}].$$

Under these conditions the transmission gates operate as ideal switches. The voltage U_{out} is equal to U_2. No current will flow:

$$I_{in1} = 0$$
$$I_{out} = 0.$$

In an under/over voltage operation condition the following input voltage conditions are considered as under and over voltage conditions:

Under voltage:

$$-V_{THn} + V_{SS} \leq U_1 \leq V_{SS}$$

Over voltage:

$$V_{CC} \leq U_1 \leq V_{CC} + |V_{THp}|$$

(V_{THn}, V_{THp} are threshold voltages of p- and n channel transistors)

The voltage U_2 is:

$$U_2 = [V_{SS};\ V_{CC}].$$

Under these conditions the first transmission gate FT_0 in channel IN_0 does not work as an ideal switch. The current I_{in1} is bypassed to V_{SS} level or V_{CC} level by using the bypass circuit 50 or 60. The second transmission gate ST_0 is implemented in order not to change the U_{out} voltage. In case of an over/under voltage condition the bypass circuit 50 reduces the input voltage for the second transmission gate ST_0, so that no over voltage condition occurs at the second transmission gate ST_0 and the bypass circuit 60 increases the input voltage for the second transmission gate, so that no under voltage condition occurs at the second transmission gate ST_0. Therefore, the second transmission gate will work again as an ideal switch. As a result no current flows between IN_0 and IN_1 and the voltage U_{out} is equal to the input voltage U_2, i.e.

$$\begin{aligned} |I_{in1}| &\geq 0 \\ |I_{in2}| &= 0 \\ |I_{out}| &= 0 \\ U_{out} &= U_2. \end{aligned}$$

An additional circuit senses either the voltage in front of FT_0 or between FT_0 and ST_0 and switches on either the bypass circuit to V_{CC} in case of under voltage or the bypass circuit to V_{SS} in case of over voltage. This is necessary to avoid a shortcut between V_{CC} and V_{SS} via the two bypass circuits. The combination of the bypass circuit and the sense circuit forms a bypass and sense circuit.

In a further development the bypass and sense circuit contains elements to control the potential between FT_0 and ST_0.

Fig. 3 shows a specific embodiment of the multiplexer circuit according to Fig. 2. For each channel the pull-down bypass circuit 50 is realized with an NMOS transistor 80, 81 and the pull-up bypass circuit is realized with a PMOS transistor 90, 91, respectively. The NMOS transistor will be used as over voltage protection and the PMOS transistor will be used as under voltage protection on channels that are not selected.

A control circuit for the bypass circuits comprises NOR gates 100, 101, the output of which is connected with the gate of the NMOS transistor 80, 81, respectively. The control circuit further comprises NAND gates 110, 111, the output of which is connected with the gate of the PMOS transistor 90, 91, respectively. One input of the NOR gate 100, 101 is connected with the input voltage U_1, U_2, respectively, and the other input of the NOR gate 100, 101 is connected with the select signal $SELECT_0$, $SELECT_1$. One input of the NAND gate 110, 111 is connected with the input voltage U_1, U_2, respectively., and the other input of the NAND gate 110, 111 is connected with the inverted select signal $\overline{SELECT_0}$, $\overline{SELECT_1}$. Therefore, the input signals of the control circuit are the input voltage U_1, U_2 and the select and the inverted select signals which control the transmission gates. If a channel is not selected (SELECT = 0) and an under voltage condition occurs ($U_1 < 0$ V) the PMOS transistor 90 will be switched on. If a channel is not selected (SELECT = 0) and an over voltage condition occurs ($U_1 > 5$ V), the NMOS transistor 80 will be switched on.

Fig. 4 shows a second specific embodiment of the multiplexer circuit according to Fig. 2. A control circuit for controlling the bypass circuit comprises a sense circuit for sensing a voltage in the input channel. The sense circuit and the bypass circuit in combination form a bypass and sense circuit consisting of a sense path and a bypass path. In the bypass and sense circuit to V_{SS} the sense path comprises a PMOS transistor 130, 131 in series with an NMOS transistor 120, 121. The source of the PMOS transistor 130, 131 is connected

to said first transmission gate FT_0, FT_1 and the source of the NMOS transistor 120, 121 is connected to ground level V_{SS}. The drain of the PMOS transistor 130, 131 is connected with the drain of the NMOS transistor 120, 121. The bypass path is formed of NMOS transistor 160, 161 the drain of which is connected with the output of said first transmission gate FT_0, FT_1 and the source of which is connected with V_{SS} . The gate of NMOS transistor 160, 161 is connected with the drains of the PMOS and NMOS transistors of the sense circuit. The driveability of NMOS transistor 120, 121 is very weak compared to the driveability of PMOS transistor 130, 131. For a channel that is switched off a voltage of $0.65V_{DD}$ is applied to gate of PMOS 130, 131. Both the sense path and the bypass path are switched off as long as the potential at node 70, 71 fulfils the condition $U70<0.65V_{DD}+|V_{THp}|$. When due to an over voltage at the input the voltage at node 70, 71 exceeds $U70>0.65V_{DD}+|V_{THp}|$ the sense path drives a small current to V_{SS}. Because of the big impedance of NMOS 120, 121 compared to the impedance of PMOS 130, 131 the gate voltage at the gate of bypass transistor NMOS 160, 161 increases very quickly so that this transistor changes very quickly to the conducting state. In this way a low impedance path to V_{SS} is installed when the voltage U70 is close to V_{DD}. The bypass and sense circuit to V_{SS} can be associated with an ideal switch that switches on as soon as U70 approximates V_{DD}.

The pull-up bypass and sense circuit consists of NMOS 140, 141 and PMOS 150, 151 as sense path and PMOS 170, 171 as bypass path. In the bypass path, the drain of PMOS transistor 170, 171 is connected with the output 70, 71 of said first transmission gate FT_0, FT_1 and the source is connected with power supply voltage level V_{CC}. In the sense path the source of the PMOS transistor 150, 151 is connected to power supply voltage level V_{CC} and the source of the NMOS transistor 140, 141 is connected to an output 70, 71 of said first transmission gate FT_0, FT_1 and the drains of the PMOS transistor 150, 151 and the NMOS transistor 140, 141 are

connected to each other. The gate of the PMOS transistor 170, 171 is connected with the drains of the PMOS and NMOS transistors of the sense path. The bypass and sense circuit works in an analogue way for undervoltage.

Measurements on real chips prove that a subthreshold current via closed FT_0 can occur also for valid input voltages $V_{SS}<U1<V_{DD}$ dependent on the voltage drop between drain and source of FT_0. If this voltage drop is significant leakage is likely to occur due to the fact that the V_{DD} level in the chip (and at the gate of FT_0) is a little bit less than the V_{DD} level applied from externally and due to the big width of FT_0, which is necessary to achieve a small impedance if the input is active ADC input channel. The proposed bypass and sense circuits keep the voltage drop on FT_0 as small as possible and thus limit the subthreshold current into the pad. The reason is that both bypass and sense circuits are switched off for potentials U70 in the range $0.35V_{DD}-V_{THn}<U70<0.65V_{DD}+|V_{THp}|$, i.e. currents via FT_0 can only flow if one of the conditions $U70>0.65V_{DD}+|V_{THp}|$ or $U70<0.35V_{DD}-V_{THn}$ is fulfilled.

A small pad input leakage current is an important quality criteria for the IO circuit of an integrated circuit.

Of course, each of the embodiments according to Figs. 1 to 4 may comprise not only two but a plurality of input channels and each channel may have the pull-up and/or pull-down circuits and the second transmission gates as described above.

An ADC circuit according to the invention comprises a multiplexer circuit according to the embodiments of Figs. 1 to 4 where the output voltage U_{OUT} of the multiplexer is the input voltage for the ADC. The accuracy of such an ADC can be as good as without over/undervoltage, i.e. the over/undervoltage has no influence to the conversion result (e.g. in case of an 8-bit ADC the accuracy is +/-2 LSB with or without over/undervoltage).